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INTEGRATED SEMICONDUCTOR MEMORY DEVICE AND ITS DRIVING METHOD
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Abstract: PURPOSE: To realize a FIFO operation and memory address designation which can freely select blocks at the time of reading or writing data.

CONSTITUTION: A write intermediate memory 10 where a write pointer 11 is made to correspond to a an input buffer 13, a read intermediate memory 20 where a read pointer 21 is made to correspond to an output buffer 23 and a controller 2 are provided. A read column address decoder 22 controlling the read pointer 21 is made to correspond to the read intermediate memory 20. The decoder 22 is connected to a read address register 25 through a read address control unit 24. A row address decoder 8 is provided in a memory control circuit 3 or a memory range 1 and it can be controlled by a read address control unit 24.

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